



# IGC70T120T6RL

## IGBT4 Low Power Chip

### FEATURES:

- 1200V Trench + Field Stop technology
- low switching losses
- positive temperature coefficient
- easy paralleling

### This chip is used for:

- low / medium power modules

### Applications:

- low / medium power drives



Chip Type	V <sub>CE</sub>	I <sub>CN</sub>	Die Size	Package
IGC70T120T6RL	1200V	75A	9.12 x 7.71 mm <sup>2</sup>	sawn on foil

### MECHANICAL PARAMETER

Raster size	9.12 x 7.71	mm <sup>2</sup>
Emitter pad size (incl. gate pad)	7.61 x 6.24	
Gate pad size	1.31 x 0.81	
Area total / active	70.3 / 51.6	
Thickness	115	µm
Wafer size	150	mm
Flat position	90	grd
Max.possible chips per wafer	200	
Passivation frontside	Photoimide	
Pad metal	3200 nm AlSiCu	
Backside metal	Ni Ag –system suitable for epoxy and soft solder die bonding	
Die bond	Electrically conductive glue or solder	
Wire bond	Al, <500µm	
Reject ink dot size	Ø 0.65mm ; max 1.2mm	
Recommended storage environment	Store in original container, in dry nitrogen, < 6 month at an ambient temperature of 23°C	



# IGC70T120T6RL

## MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Collector-Emitter voltage, $T_j=25\text{ }^\circ\text{C}$	$V_{CE}$	1200	V
DC collector current, limited by $T_{jmax}$	$I_C$	<sup>1)</sup>	A
Pulsed collector current, $t_p$ limited by $T_{jmax}$	$I_{Cpuls}$	225	A
Gate-Emitter voltage	$V_{GE}$	$\pm 20$	V
Operating junction temperature	$T_j$	-40 ... +175	$^\circ\text{C}$
Short circuit data <sup>2)</sup> $V_{GE} = 15\text{V}$ , $V_{CC} = 800\text{V}$ , $T_{vj} = 150^\circ\text{C}$	$t_p$	10	$\mu\text{s}$
Reverse bias safe operating area <sup>2)</sup> (RBSOA)	$I_{Cmax} = 150\text{A}$ , $V_{CEmax} = 1200\text{V}$ , $T_{vjmax} = 150^\circ\text{C}$		

<sup>1)</sup> depending on thermal properties of assembly

<sup>2)</sup> not subject to production test - verified by design/characterization

## STATIC CHARACTERISTICS (tested on wafer), $T_j=25\text{ }^\circ\text{C}$

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-Emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0\text{V}$ , $I_C=3\text{mA}$	1200			V
Collector-Emitter saturation voltage	$V_{CE(sat)}$	$V_{GE}=15\text{V}$ , $I_C=75\text{A}$	1.6	1.85	2.1	
Gate-Emitter threshold voltage	$V_{GE(th)}$	$I_C=3\text{mA}$ , $V_{GE}=V_{CE}$	5.0	5.8	6.5	
Zero gate voltage collector current	$I_{CES}$	$V_{CE}=1200\text{V}$ , $V_{GE}=0\text{V}$			10	$\mu\text{A}$
Gate-Emitter leakage current	$I_{GES}$	$V_{CE}=0\text{V}$ , $V_{GE}=20\text{V}$			600	nA
Integrated gate resistor	$R_{Gint}$			10		$\Omega$

## ELECTRICAL CHARACTERISTICS (not subject to production test - verified by design/characterization)

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Input capacitance	$C_{iss}$	$V_{CE}=25\text{V}$ , $V_{GE}=0\text{V}$ , $f=1\text{MHz}$		4400		pF
Output capacitance	$C_{oss}$			290		
Reverse transfer capacitance	$C_{rss}$			235		



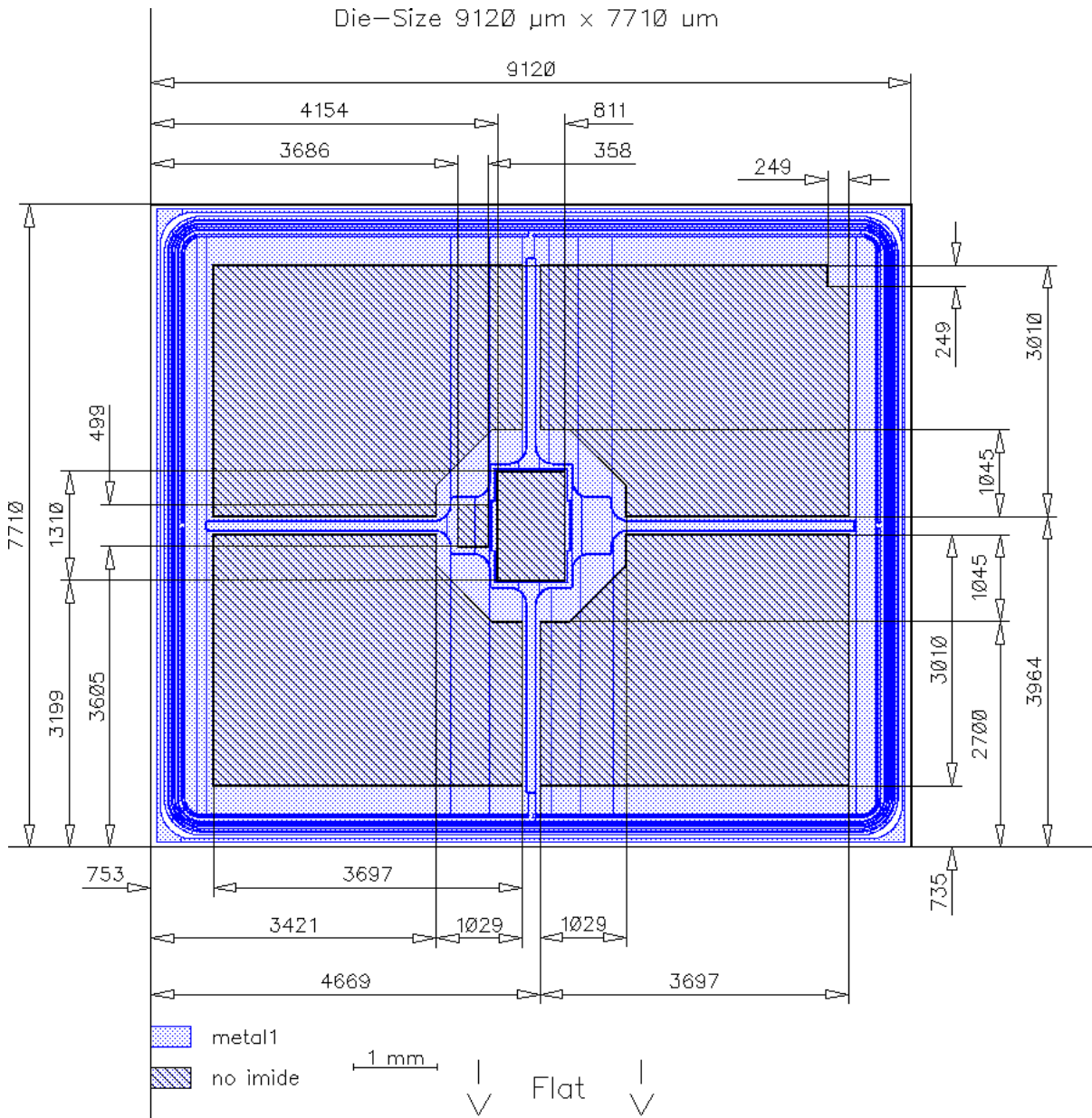
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**SWITCHING CHARACTERISTICS** inductive load (not subject to production test - verified by design /characterization)

Parameter	Symbol	Conditions <sup>1)</sup>	Value			Unit
			min.	typ.	max.	
Turn-on delay time	$t_{d(on)}$	$T_j = 125^\circ\text{C}$ $V_{CC} = 600\text{V},$ $I_C = 75\text{ A},$ $V_{GE} = -15/15\text{V},$ $R_G = \text{---}\Omega$		tbd		ns
Rise time	$t_r$			tbd		
Turn-off delay time	$t_{d(off)}$			tbd		
Fall time	$t_f$			tbd		

<sup>1)</sup> values also influenced by parasitic L- and C- in measurement and package.

## CHIP DRAWING





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## FURTHER ELECTRICAL CHARACTERISTICS

This chip data sheet refers to the device data sheet	tbd	
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## DESCRIPTION

AQL 0,65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

Test-Normen Villach/Prüffeld

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